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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,545	RABKIN ET AL.	
	Examiner	Art Unit	AW
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 17 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 17 recites "a control gate comprising a third polysilicon layer... ; ... ; the fourth polysilicon layer having a doping concentration which decreases in a direction away from am interface between the third and fourth polysilicon layers. The application, at best, discloses especially in Fig. 5 that the undoped layers of the *floating gate* has an impurity concentration gradually reduces at the boundaries between the doped and the undoped polysilicon layers and reaches it's the lowest concentration level at the interface between the undoped polysilicon layer and the corresponding the insulating layers after the thermal cycles on page 7, lines 15-28. However, the application does not disclose explicitly the undoped layer of the *control gate* has the same characteristics of the undoped layer of the floating gate.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 recites "a floating gate comprising a first polysilicon layer over the first insulating layer; and a second polysilicon layer over and in contact with the first polysilicon layer, ...; a second insulating layer over and *in contact with* the first polysilicon layer; and a control gate comprising a fourth polysilicon layer over and *in contact with* the second insulating layer..." Throughout the specification, especially Figure 3a shows the floating gate comprising a first insulating layer (304), first polysilicon layer (306-a), a second polysilicon layer (306-b) and a second insulating layer (308) in contact with the second polysilicon layer. And a third polysilicon layer (310-a) of the control gate is in contact with the second insulating layer (308). Therefore, the first polysilicon layer cannot be in contact with the second insulating layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-25, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (US 5840607), hereafter Yeh in view of and Park (US 6107169).

Regarding claim 17, insofar as understood, Fig. 4 of Yeh shows a semiconductor

transistor comprising:

a first insulating layer (20) over a substrate region; a floating gate comprising a first polysilicon layer (24) over the first insulating layer; and a second polysilicon layer (26) over and in contact with the first polysilicon layer;

a second insulating layer (28, 30, 32) over and in contact with the first polysilicon layer; and

a control gate comprising a third polysilicon layer (34) over and in contact with the second insulating layer.

Yeh teaches substantially the entire claimed structure except a control gate having another polysilicon layer beneath the polysilicon layer. Fig. 3d of Park shows an undoped polysilicon portion (34; col. 7, lines 12-30) of the control gate (26'). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Park into the device of Yeh in order to have another polysilicon layer, especially an undoped layer in the control gate to avoid the surface roughness on the gate.

Regarding the limitations of "the first polysilicon layer having a predetermined doping concentration and the second polysilicon layer having a doping concentration which decreases in a direction away from an interface between the first and second polysilicon layers" and "the fourth polysilicon layer having a predetermined doping concentration and the third polysilicon layer having a doping concentration which decreases in a direction away from an interface between the first and second polysilicon layers, first it is obvious that the first and fourth polysilicon layers of Yeh have a

predetermined doping concentration since these layers are doped. Second, the limitation of "the second polysilicon layer having a doping concentration which decreases in a direction away from an interface between the first and second polysilicon layers" merely describes the inherent characteristics of the undoped polysilicon layers after the thermal cycle. Note that Yeh's second layer of the floating gate is undoped polysilicon layer which is formed through a thermal process (col. 3, lines 39-44) and the undoped layer of the Park's control gate would be thermally processed to diffuse the impurity dopant to the floating gate.

Regarding claim 18, Fig. 4 of Yeh shows the floating gate further comprises a fifth polysilicon layer (22)over and in contact with the first insulating layer(20).

The limitations of "the fifth polysilicon layer having a doping concentration which decreases in a direction away from an interface between the first and fifth polysilicon layers" have been discussed above in claim 17. In detail, this limitation merely recites an inherent characteristics of the fifth polysilicon layer of Yeh's floating gate which is undoped and processed thermally.

Regarding claim 19, Fig. 4 of Yeh shows a device comprising wherein the first insulating layer (20) is a tunnel oxide layer (col. 2, line 22) and the second insulting layer (28, 30, 32) is a composite oxide-nitride-oxide dielectric layer (col. 2, lines 25-29).

Regarding claim 20, Yeh discloses that a thickness of the first polysilicon layer is greater than a thickness of each of the second and fifth polysilicon by a factor in the range of two to four (col. 3, lines 23-45). Park discloses that a thickness of the fourth polysilicon layer is greater than a thickness of the third polysilicon layer (col. 6, line 63-col.7, line 21). Yeh and Park do not explicitly disclose a recited range of thickness of the

third polysilicon layer. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a thickness of the nitride layer recited in pending claim, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 21, Fig. 4 of Yeh shows insulating spacers(42) along sidewalls of the stack made up of the first insulting layer, the floating gate, the second insulating layer, and the control gate; and source and drain regions (44)in the substrate.

Regarding claim 22, Fig. 4 of Yeh shows the first polysilicon layer is in-situ doped with impurities (co. 3, lines 32-36).

In addition, note that "in-situ" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 23, Fig. 4 of Yeh shows a stacked gate.

Regarding claim 24, Yeh discloses that the first polysilicon layer has a doping concentration and a thickness greater than each of the second and the fifth polysilicon layers and the smaller grain size of undoped polysilicon layer reduces the impurity diffusion from the overlying doped polysilicon thus, preventing the gate oxide from degrading (col.3, lines 22- 45).

In addition, the limitation of "so as to prevent polysilicon depletion in the control gate in pending claim" is an operating function of device rather than a structure of device and is not structurally distinguishing.

Regarding claim 25, Yeh discloses the device is EEPROM (col. 1, lines 24-25).

Claims 17- 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Poon et al (US 4978626).

Regarding claim 17, Fig. 4 of Yeh teaches each element of the claim except for a control gate having an undoped polysilicon layer beneath a doped polysilicon layer. Figure 1 H of Poon teaches a gate electrode having an undoped polysilicon layer beneath a doped polysilicon layer. The paragraph spanning columns 5 and 6 of Poon explains the reasons why the undoped polysilicon layer is advantageous. It would have been obvious to include an undoped polysilicon layer beneath the doped polysilicon layer of the Yeh control gate, for the reasons noted by Poon.

Regarding claims 18-19, 21-22, 23, and 25, the recited structure is shown in Figure 4 of Yeh.

Regarding claims 20 and 24, layer 17 of Poon Figure1 H is shown as having a thickness of more than two times the thickness of layer 15.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi
November 5, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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